

DC BIAS CONTROL CIRCUIT, OPTICAL RECEIVER, AND
DC BIAS CONTROL METHOD

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a DC bias control circuit for, an optical receiver for, and a DC bias control method of reducing the amount of jitter in regenerated data.

Description of the Prior Art

10 Fig. 12 is a block diagram showing the structure of a prior art optical receiver disclosed in Japanese patent application publication (TOKKAIHEI) No. 11-284572. In the figure, reference numeral 1 denotes a light receiving element for converting an incoming optical signal into an electrical current signal, reference numeral 2 denotes a preamplifier for converting the electrical current signal which flows through the light receiving element 1 into a voltage signal, reference numeral 3 denotes a capacitor for blocking a DC component of the voltage signal from the preamplifier 2 and for allowing an AC component of the voltage signal to pass therethrough, and reference numeral 4 denotes a data regeneration and clock recovery circuit for reshaping and regenerating data from the AC component of the voltage signal which passes through the capacitor 3, and for recovering a clock from the AC component of the voltage signal.

25 In operation, the light receiving element 1 converts an incoming optical signal into an electrical current signal, and the preamplifier 2 then converts the electrical current signal which flows through the light receiving element 1 into a voltage signal and outputs the voltage signal. When the power of the
30 incoming optical signal grows, a distortion might be generated

in the output signal of the preamplifier 2 depending on the characteristics of the light receiving element 1 and the characteristics of the preamplifier 2, and therefore the level of a crossing point (or eye crossing) of an eye diagram of the signal input to the data regeneration and clock recovery circuit 4, at which the rising and falling edges of pulses included in the incoming signal cross each other, might be shifted from the DC level (i.e., the mean level of the incoming signal) upwardly or downwardly.

10 In general, the data regeneration and clock recovery circuit 4 receives a differential input, and the AC component of the voltage signal from the capacitor 3 to which a DC bias is applied is input to a normal-phase side of the data regeneration and clock recovery circuit 4 and a threshold voltage used for
15 determining whether the regenerated data is 0 or 1 is supplied to an opposite-phase side of the data regeneration and clock recovery circuit 4. The threshold voltage supplied to the opposite-phase side is equal to the DC bias applied to the normal-phase side.

20 Figs. 13A and 13B are diagrams each showing the waveforms of an incoming optical signal applied to and data regenerated by the data regeneration and clock recovery circuit 4. Fig. 13A shows a case where the input power of the optical signal has a normal level and no distortion is generated in the output signal of the preamplifier 2, and Fig. 13B shows a case where
25 the input power of the optical signal indicates has a large level and a distortion is generated in the output signal of the preamplifier 2.

As shown in Fig. 13A, when no distortion is generated in
30 the output signal of the preamplifier 2 and the output signal

has an excellent waveform, the waveform of the output signal can be symmetric with respect to the DC level and the level of the crossing point of the eye diagram of the output signal at which the rising and falling edges of the waveform cross each other corresponds to the mean level of the waveform. Therefore, since the crossing point thus corresponds to the threshold voltage, when a waveform 101 is input to the data regeneration and clock recovery circuit 4, the data regeneration and clock recovery circuit 4 regenerates data having a waveform 103, and when a waveform 102 is input, the data regeneration and clock recovery circuit 4 regenerates data having a waveform 104. As a result, the rising and falling edges of the regenerated data waveform 103 coincide with the falling and rising edges of the regenerated data waveform 104, respectively, and therefore no time difference Δt occurs between them and no jitter occurs in the regenerated data.

However, as shown in Fig. 13B, when a distortion is generated in the output signal of the preamplifier 2, if the crossing point of the eye diagram is shifted upwardly, the mean level of the waveform is increased and therefore the entire of the waveform is seemed to be lowered with respect to the DC level. The crossing point of the eye diagram might be shift downwardly according to the characteristic of the preamplifier 2 instead of being shifted upwardly as shown in Fig. 13B. In Fig. 13 B in which the crossing point of the eye diagram is shifted upwardly with respect to the threshold voltage, when a waveform 105 is input to the data regeneration and clock recovery circuit 4, the data regeneration and clock recovery circuit 4 regenerates data having a waveform 107, and when a waveform 106 is input, the data regeneration and clock recovery circuit 4 regenerates

data having a waveform 108. As a result, the rising and falling edges of the regenerated data waveform 107 do not coincide with the falling and rising edges of the regenerated data waveform 108, respectively, and therefore a time difference Δt occurs between them and jitter occurs in the regenerated data.

A problem with the prior art optical receiver constructed as mentioned above is that when a distortion occurs in a signal input to the data regeneration and clock recovery circuit 4, and therefore the crossing point of an eye diagram of the input signal at which the rising and falling edges of the input signal cross each other is shifted from the mean level of the input signal, jitter can occur in the regenerated data.

SUMMARY OF THE INVENTION

The present invention is proposed to solve the above-mentioned problems, and it is therefore an object of the present invention to provide a DC bias control circuit, an optical receiver, and a DC bias control method capable of reducing the amount of jitter in regenerated data even if a distortion occurs in an input signal and therefore the crossing points where the rising and falling edges of two possible waveforms of the signal cross each other are shifted from the mean level of each of the two possible waveforms.

In accordance with an aspect of the present invention, there is provided a DC bias control circuit for controlling a DC bias added to an AC component of an output signal delivered from an amplifier to a data regeneration circuit that regenerates data from the AC component of the output signal from the amplifier based on a predetermined threshold voltage, wherein the DC bias control circuit controls the DC bias based on a HIGH level, a

DC level, and a LOW level of the signal output from the amplifier.

In accordance with another aspect of the present invention, the DC bias control circuit comprises: a HIGH level detector for detecting a HIGH level of the output signal from the amplifier; a DC level detector for detecting a DC level of the output signal from the amplifier; a LOW level detector for detecting a LOW level of the output signal from the amplifier; a first subtracting circuit for determining a first subtraction result by subtracting the DC level from the HIGH level; a second subtracting circuit for determining a second subtraction result by subtracting the LOW level from the DC level; a third subtracting circuit for determining a third subtraction result by subtracting the second subtraction result from the first subtraction result; and a correction circuit for correcting the DC bias by weighting the third subtraction result according to characteristics of the amplifier, and by determining a difference between a level of a crossing point of an eye diagram of the output signal from the amplifier, at which rising and falling edges of pulses included in the output signal from the amplifier cross each other, and the DC level.

In accordance with a further aspect of the present invention, there is provided an optical receiver comprising: a light receiving element for converting an incoming optical signal into an electrical current signal; a preamplifier for converting the electrical current signal which flows through the light receiving element into a voltage signal; and a data regeneration and clock recovery circuit for applying a DC bias to an AC component of the voltage signal from the preamplifier, and for reshaping and regenerating data and recovering a clock from the AC component based on a predetermined threshold voltage,

wherein the optical receiver controls the DC bias based on a HIGH level, a DC level, and a LOW level of the output signal from the preamplifier.

In accordance with another aspect of the present invention,

5 the optical receiver further comprises: a HIGH level detector for detecting a HIGH level of the output signal from the preamplifier; a DC level detector for detecting a DC level of the output signal from the preamplifier; a LOW level detector for detecting a LOW level of the output signal from the

10 preamplifier; a first subtracting circuit for determining a first subtraction result by subtracting the DC level from the HIGH level; a second subtracting circuit for determining a second subtraction result by subtracting the LOW level from the DC level; a third subtracting circuit for determining a third subtraction

15 result by subtracting the second subtraction result from the first subtraction result; and a correction circuit for correcting the DC bias by weighting the third subtraction result according to characteristics of the light receiving element and characteristics of the amplifier, and by determining a difference

20 between a level of a crossing point of an eye diagram of the output signal from the preamplifier, at which rising and falling edges of pulses included in the output signal from the preamplifier cross each other, and the DC level.

In accordance with a further aspect of the present

25 invention, there is provided a method of controlling a DC bias added to an AC component of an output signal delivered from an amplifier to a data regeneration circuit that regenerates data from the AC component of the output signal from the amplifier based on a predetermined threshold voltage, the method comprising

30 the steps of: detecting a HIGH level of the output signal from

the amplifier; detecting a DC level of the output signal from the amplifier; detecting a LOW level of the output signal from the amplifier; determining a first subtraction result by subtracting the DC level from the HIGH level; determining a second subtraction result by subtracting the LOW level from the DC level;
 5 determining a third subtraction result by subtracting the second subtraction result from the first subtraction result; and correcting the DC bias by weighting the third subtraction result according to characteristics of the amplifier, and by determining
 10 a difference between a level of a crossing point of an eye diagram of the output signal from the amplifier, at which rising and falling edges of pulses included in the output signal from the amplifier cross each other, and the DC level.

Accordingly, the present invention offers an advantage
 15 of being able to reduce the amount of jitter in regenerated data.

Further objects and advantages of the present invention will be apparent from the following description of the preferred embodiments of the invention as illustrated in the accompanying drawings.

20

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of an optical receiver according to a first embodiment of the present invention;

25 Fig. 2 is a circuit diagram showing the structure of a High level detection circuit of the optical receiver according to the first embodiment of the present invention;

Fig. 3 is a circuit diagram showing the structure of a Low level detection circuit of the optical receiver according
 30 to the first embodiment of the present invention;

Fig. 4A is a block diagram showing the structure of a circuit including the function of the High level detection circuit and the function of the Low level detection circuit in the optical receiver according to the first embodiment of the present invention;

Fig. 4B is a diagram showing a histogram of sampled values of an analog-to-digital converted output signal of a preamplifier of the optical receiver according to the first embodiment of the present invention;

Fig. 5 is a circuit diagram showing the structure of an example of a DC level detection circuit of the optical receiver according to the first embodiment of the present invention;

Fig. 6 is a circuit diagram showing the structure of another example of the DC level detection circuit of the optical receiver according to the first embodiment of the present invention;

Figs. 7A and 7B are diagrams each showing the waveform of a signal input to a data regeneration and clock recovery circuit of the optical receiver according to the first embodiment of the present invention when an output signal of a preamplifier has a distortion;

Fig. 8 is a diagram showing an example of a weighting correction characteristic of a correction circuit of the optical receiver according to the first embodiment of the present invention;

Fig. 9 is a diagram showing a relationship between the weighting correction characteristic of the correction circuit of the optical receiver according to the first embodiment of the present invention and actual characteristics of a light receiving element and the preamplifier;

Fig. 10 is a diagram showing a relationship between the

weighting correction characteristic of the correction circuit of the optical receiver according to the first embodiment of the present invention and the actual characteristics of the light receiving element and the preamplifier;

5 Fig. 11 is a block diagram showing the structure of a DC bias control circuit according to a second embodiment of the present invention;

 Fig. 12 is a block diagram showing the structure of a prior art photoreceiver; and

10 Figs. 13A and 13B are diagrams each showing the waveforms of an input optical signal applied to and data regenerated by a data regeneration and clock recovery circuit of the prior art photoreceiver.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS Embodiment 1.

 Fig. 1 is a block diagram showing the structure of an optical receiver according to a first embodiment of the present invention. In Fig. 1, a light receiving element 1, a preamplifier 2, a capacitor 3, and an data regeneration and clock recovery circuit 4 have the same structures as those of the prior art optical receiver shown in Fig. 12, respectively. The explanation of those components designated by the same reference numerals will be omitted hereafter. Reference numeral 11 denotes a High level detection circuit for detecting a High level of an output signal output from the preamplifier 2, reference numeral 12 denotes a DC level detection circuit for detecting a DC level of the output signal output from the preamplifier 2, and reference numeral 13 denotes a Low level detection circuit for detecting a Low level of the output signal output from the preamplifier

20

25

30

2.

Furthermore, in Fig. 1, reference numeral 14 denotes a subtracting circuit (first subtracting circuit) for determining a first subtraction result by subtracting the DC level of the output signal detected by the DC level detection circuit 12 from the High level of the output signal detected by the High level detection circuit 11, and reference numeral 15 denotes a subtracting circuit (second subtracting circuit) for determining a second subtraction by subtracting the Low level of the output signal detected by the Low level detection circuit 13 from the DC level of the output signal detected by the DC level detection circuit 12.

In addition, in Fig. 1, reference numeral 16 denotes a subtracting circuit (third subtracting circuit) for determining a third subtraction result by subtracting the second subtraction result determined by the subtracting circuit 15 from the first subtraction result determined by the subtracting circuit 14, and reference numeral 17 denotes a correction circuit for weighting the third subtraction result determined by the subtracting circuit 16 according to characteristics of the light receiving element 1 and characteristics of the preamplifier 2, and for determining a difference ΔV between the level of a crossing point (or eye crossing) of an eye diagram of the output signal from the preamplifier 2, at which the rising and falling edges of pulses included in the output signal from the preamplifier 2 cross each other, and the DC level, so as to reduce a DC bias applied to a normal-phase side of an input of the data regeneration and clock recovery circuit 4 by only ΔV .

Fig. 2 is a circuit diagram showing the structure of the High level detection circuit 11. The High level detection

circuit 11 detects the High level of the output signal of the preamplifier 2 by using a half-wave rectification circuit that consists of a capacitor 21, a resistor 22, a diode 23, and a capacitor 24. Fig. 3 is a circuit diagram showing the structure of the Low level detection circuit 13. The Low level detection circuit 13 detects the Low level of the output signal of the preamplifier 2 by using a half-wave rectification circuit that consists of a capacitor 25, a resistor 26, a diode 27, and a capacitor 28.

Fig. 4A is a block diagram showing the structure of a circuit including the function of the High level detection circuit 11 and the function of the Low level detection circuit 13. In the figure, reference numeral 31 denotes an AD conversion circuit for converting the output signal from the preamplifier 2 into an equivalent digital value, reference numeral 32 denotes a control circuit for sampling the converted digital value at predetermined intervals determined by sampling pulses applied thereto, and for acquiring a histogram of sampled values so as to determine the level of the largest number of accumulations as the High level or Low level of the output signal, and reference numeral 33 denotes a memory for accumulating and storing the sampled values on a level-by-level basis under control of the control circuit 32.

Fig. 5 is a circuit diagram showing the structure of an example of the DC level detection circuit 12. The DC level detection circuit 12 includes two resistors 41 and 42 for voltage-dividing the output signal of the preamplifier 2 having a DC level of V_{dc} , and an amplifier 43 for blocking high-frequency components of the voltage-divided output signal and for amplifying low-frequency components of the voltage-divided

output signal.

Fig. 6 is a circuit diagram showing the structure of another example of the DC level detection circuit 12. The DC level detection circuit 12 includes a capacitor 44 for blocking DC components of the output signal of the preamplifier 2 and a resistor 45 connected to a power supply having a DC level of Vdc. When using the DC level detection circuit 12 shown in Fig. 6, there is a necessity to use the High level detection circuit 11 shown in Fig. 2 and the Low level detection circuit 13 shown in Fig. 3, they having a common power supply of Vdc.

In operation, the light receiving element 1 and the preamplifier 2 shown in Fig. 1 operate in the same way that those of the prior art photo receiver shown in Fig. 12 do. The High level detection circuit 11 shown in Fig. 2 performs half-wave rectification on the output signal of the preamplifier 2 having a DC level of Vdc, as can be seen from the waveforms of an input and output of the High level detection circuit 11, so as to detect the High level of the output signal of the preamplifier 2.

Similarly, the Low level detection circuit 13 shown in Fig. 3 performs half-wave rectification on the output signal of the preamplifier 2 having a DC level of Vdc, as can be seen from the waveforms of an input and output of the Low level detection circuit 13, so as to detect the Low level of the output signal of the preamplifier 2.

In addition, in the circuit shown in Fig. 4A including the function of the High level detection circuit 11 and the function of the Low level detection circuit 13, the AD conversion circuit 31 converts the output signal from the preamplifier 2 into an equivalent digital value, and the control circuit 32 then samples the converted digital value at predetermined

intervals determined by sampling pulses whose repetition rate is greater than a data transmission rate at which data are transmitted, and accumulates and stores sampled values in the memory 33 on a level-by-level basis. The control circuit 32
 5 acquires a histogram of the sampled values accumulated on a level-by-level basis, as shown in Fig. 4B, so as to determine the level of the largest number of accumulations as the High level or Low level of the output signal of the preamplifier 2.

The DC level detection circuit 12 detects the DC level
 10 of the output signal of the preamplifier 2. In the DC level detection circuit 12 shown in Fig. 5, the output signal from the preamplifier 2 having a DC level of V_{dc} is voltage-divided by the resistors 41 and 42 and is then input to the amplifier 43. Assuming that the resistors 41 and 42 have resistance values
 15 R_1 and R_2 , respectively, the voltage-divided DC level V_0 is given by the following equation (1).

$$V_0 = V_{dc} \times R_2 / (R_1 + R_2) \quad (1)$$

20 The voltage-divided DC level V_0 is then input to the amplifier 43. The amplifier 43 blocks high-frequency components and amplifies low-frequency components, and has a gain G set to $(R_1 + R_2) / R_2$. Therefore, the output of the amplifier 43 has a voltage V_1 given by the following equation (2).

$$V_1 = V_0 \times G = V_0 \times (R_1 + R_2) / R_2 \quad (2)$$

Substituting the above-mentioned equation (1) into the above-mentioned equation (2) yields the output voltage V_1 of
 30 the amplifier 43 given by the following equation (3).

$$\begin{aligned}
 V1 &= V0 \times (R1+R2) / R2 \\
 &= Vdc \times (R2 / (R1+R2)) \times ((R1+R2) / R2) \\
 &= Vdc
 \end{aligned}
 \tag{3}$$

5

In other words, the DC level V_{dc} of the output signal of the preamplifier 2 is detected.

In the DC level detection circuit 12 shown in Fig. 6, the capacitor 44 blocks the DC level from the preamplifier 2, and a DC level V_{dc} newly given by a power supply is output from the DC level detection circuit 12 to the subtracting circuits 14 and 15, just as it is. The DC level V_{dc} from the power supply is equal to the power supply V_{dc} of the High level detection circuit 11 shown in Fig. 2 and is also equal to the power supply V_{dc} of the Low level detection circuit 13 shown in Fig. 3.

In Fig. 1, the subtracting circuit 14 subtracts the DC level detected by the DC level detection circuit 12 from the High level detected by the High level detection circuit 1 so as to calculate a voltage difference ΔV_{high} between the High level and the DC level, which is the first subtraction result. The subtracting circuit 15 subtracts the Low level detected by the Low level detection circuit 13 from the DC level detected by the DC level detection circuit 12 so as to calculate a voltage difference ΔV_{low} between the DC level and the Low level, which is the second subtraction result. The subtracting circuit 16 subtracts ΔV_{low} which is the second subtraction result from ΔV_{high} which is the first subtraction result so as to calculate $(\Delta V_{high} - \Delta V_{low})$, which is the third subtraction result.

The correction circuit 17 weights $(\Delta V_{high} - \Delta V_{low})$ which is the third subtraction result from the subtracting circuit

16 according to input/output characteristics of the light
 receiving element 1 and input/output characteristics of the
 preamplifier 2. The correction circuit 17 then determines a
 difference ΔV between the level of the crossing point of an
 5 eye diagram of the input wave applied to the data regeneration
 and clock recovery circuit 4, at which the rising and falling
 edges of pulses included in the input wave cross each other,
 and the DC level, so as to reduce the DC bias applied to the
 normal-phase side of the input of the data regeneration and clock
 10 recovery circuit 4 by only ΔV . Thus, the level of the crossing
 point of the eye diagram, at which the rising and falling edges
 of pulses included in the input wave applied to the data
 regeneration and clock recovery circuit 4 cross each other, can
 be matched with the threshold voltage, or the difference between
 15 the level of the crossing point and the threshold voltage can
 be reduced.

Figs. 7A and 7B are diagrams each showing the waveform
 of the input of the data regeneration and clock recovery circuit
 4 when the output signal of the preamplifier 2 has a distortion.
 20 Fig. 7A shows the waveform of the input without correction of
 the DC bias, and Fig. 7B shows the waveform of the input with
 correction of the DC bias. When no correction is performed on
 the DC bias, since there is a difference ΔV between the level
 of the crossing point and the DC level (i.e. threshold voltage),
 25 as shown in Fig. 7A, jitter occurs in the data output from the
 data regeneration and clock recovery circuit 4, as in the prior
 art case of Fig. 13B.

On the other hand, as shown in Fig. 7B, the correction
 circuit 17 can reduce the DC bias applied to the normal-phase
 30 side of the input of the data regeneration and clock recovery

circuit 4 by only ΔV so as to make the level of the crossing point of the eye diagram of the input wave match with the threshold voltage. Therefore, when a waveform 111 is input to the data regeneration and clock recovery circuit 4, data having a waveform 113 is regenerated by the data regeneration and clock recovery circuit 4. On the other hand, when a waveform 112 is input to the data regeneration and clock recovery circuit 4, data having a waveform 114 is regenerated by the data regeneration and clock recovery circuit 4. As a result, the rising and falling edges of the regenerated data waveform 113 coincide with the falling and rising edges of the regenerated data waveform 114, respectively, and therefore a time difference Δt does not occur between them and no jitter occurs in the regenerated data.

Next, a description will be made as to the weighting which is performed on $(\Delta V_{high} - \Delta V_{low})$ according to the input/output characteristics of the light receiving element 1 and the input/output characteristics of the preamplifier 2. Fig. 8 is a diagram showing an example of a weighting correction characteristic of the correction circuit 17, and shows a relationship between $(\Delta V_{high} - \Delta V_{low})$ and (the level of the crossing point-DC level = ΔV) when the output signal of the preamplifier 2 has a distortion. In Fig. 8, a region in the positive horizontal axis shows a correction characteristic when the output signal of the preamplifier 2 has a distortion and the level of the crossing point of the eye diagram of the input wave is shifted downwardly, i.e., decreased, and another region in the negative horizontal axis shows a correction characteristic when the output signal of the preamplifier 2 has a distortion and the level of the crossing point of the eye diagram of the input wave is shifted upwardly, i.e., increased.

In the correction characteristic shown in Fig. 8, it is assumed that the duration of each 1-bit data is 400psec, the amplitude of the input wave which is equal to the difference between the High level and the Low level is 400mV, and the rise time and fall time of the input wave are always constant and are 80psec. Furthermore, in Fig. 8, $(\Delta V_{high} - \Delta V_{low})$ in the horizontal axis is proportional with (the level of the crossing point - DC level = ΔV) in the vertical axis. $(\Delta V_{high} - \Delta V_{low})$, which is the third subtraction result from the subtracting circuit 16, is multiplied by a constant value (in this case, -0.75) and the multiplication result is output as ΔV from the correction circuit 17. The DC bias is decreased by only ΔV so that the level of the crossing point is made to match with the threshold voltage of the data regeneration and clock recovery circuit 4.

Fig. 9 is a diagram showing a relationship between the weighting correction characteristic of the correction circuit 17 and $(\Delta V_{high} - \Delta V_{low})$ - (the level of the crossing point - DC level = ΔV) characteristic of the input wave actually output from the preamplifier 2, which is associated with the characteristics of the light receiving element 1 of the characteristics of the preamplifier 2. In the figure, reference numeral 201 shows a plot representing an example of the characteristic of the input wave actually output from the preamplifier 2, and reference numeral 202 shows a plot representing the weighting correction characteristic of the correction circuit 17 which is the same as that shown in Fig. 8. As shown in Fig. 9, although $(\Delta V_{high} - \Delta V_{low})$ is not proportional with (the level of the crossing point - DC level = ΔV) in the characteristic of the input wave actually output

from the preamplifier 2, the difference between the level of the crossing point and the threshold voltage can be reduced by determining ΔV according to the weighting correction characteristic plot 211 that approximate the characteristic of the input wave actually output from the preamplifier 2, and therefore the jitter characteristic of the data regenerated when the output signal from the preamplifier 2 has a distortion can be improved.

Fig. 10 is a diagram showing another example of the relationship between the weighting correction characteristic of the correction circuit 17 and $(\Delta V_{\text{high}} - \Delta V_{\text{low}}) - (\text{the level of the crossing point} - \text{DC level} = \Delta V)$ characteristic of the input wave actually output from the preamplifier 2, which is associated with the characteristics of the light receiving element 1 of the characteristics of the preamplifier 2. In the figure, reference numeral 201 shows a plot representing an example of the characteristic of the input wave actually output from the preamplifier 2, reference numeral 211 shows a plot representing the weighting correction characteristic of the correction circuit 17 which is the same as that shown in Fig. 8, and reference numeral 212 shows a plot representing another weighting correction characteristic of the correction circuit 17.

As shown in Fig. 10, although $(\Delta V_{\text{high}} - \Delta V_{\text{low}})$ is not proportional with $(\text{the level of the crossing point} - \text{DC level} = \Delta V)$ in the characteristic of the input wave actually output from the preamplifier 2, the difference between the level of the crossing point and the threshold voltage can be reduced by determining ΔV according to the weighting correction characteristic plots 211 and 212 that approximate the

characteristic of the input wave actually output from the preamplifier 2 (that is, the weighting correction characteristic plot 212 is used in the region in the positive horizontal axis, whereas the other weighting correction characteristics plot 211 is used in the region in the negative horizontal axis) and therefore the jitter characteristic of the data regenerated when the output signal from the preamplifier 2 has a distortion can be improved.

Thus, the best weighting correction characteristic plot is used according to the characteristics of the light receiving element 1 and the characteristics of the preamplifier 2. Furthermore, since $(\Delta V_{high} - \Delta V_{low})$ and (the level of the crossing point - the DC level) change in proportional with the amplitude of the input wave, respectively, even when the amplitude of the input wave changes, the ratio of $(\Delta V_{high} - \Delta V_{low})$ and (the level of the crossing point - the DC level) is kept constant regardless of changes in the amplitude of the input wave. Therefore, the improvement of the jitter characteristics can be obtained regardless of the amplitude of the input wave if weighting correction characteristics as shown in Figs. 8 to 10 are provided, for example, according to the characteristics of the light receiving element 1 and the characteristics of the preamplifier 2.

As mentioned above, in accordance with the first embodiment, the optical receiver detects a HIGH level, a DC level, and a LOW level of an output signal from a preamplifier 2, determines a first subtraction result by subtracting the DC level from the HIGH level, determines a second subtraction result by subtracting the LOW level from the DC level, determines a third subtraction result by subtracting the second subtraction result from the

first subtraction result, and corrects a DC bias by weighting the third subtraction result according to characteristics of a light receiving element 1 and characteristics of the preamplifier 2, so that the level of a crossing point of an eye diagram of the output signal from the preamplifier, at which the rising and falling edges of pluses included in the output signal cross each other, is made to match with or be close to a threshold voltage, even though the input signal has a distortion and the level of the crossing point is shifted from the mean level of the input waveform. Accordingly, the present embodiment offers an advantage of being able to reduce the amount of jitter in regenerated data.

Embodiment 2.

In the above-mentioned first embodiment, the optical receiver that regenerates data and recovers a clock from an incoming optical signal is explained. The present invention is also applicable to a DC bias control circuit for use with a data regeneration circuit that receives an electrical signal which is similar to an optical signal and that regenerates data from the electrical signal.

Fig. 11 is a block diagram showing the structure of a DC bias control circuit according to a second embodiment of the present invention. In Fig. 11, reference numeral 2a denotes an amplifier for amplifying a signal applied thereto, reference numeral 4a denotes a data regeneration circuit for regenerating data from an output signal of the amplifier 2a based on a predetermined threshold voltage, and reference numeral 17a denotes a correction circuit for weighting a third subtraction result determined by a subtracting circuit 16 according to

characteristics of the amplifier 2a, and for determining a difference ΔV between the level of a crossing point of an eye diagram of the output signal from the amplifier 2a, at which the rising and falling edges of pluses included in the output
 5 signal cross each other, and a DC level, so as to reduce a DC bias applied to a normal-phase side of an input of the data regeneration circuit 4a by only ΔV .

Furthermore, in Fig. 11, reference numeral 18 denotes the DC bias control circuit for controlling the DC bias of the signal
 10 input to the data regeneration circuit 4a according to the signal output from the amplifier 2a. The DC bias control circuit includes a High level detection circuit 11, a DC level detection circuit 12, a Low level detection circuit 13, a subtracting circuit 14, a subtracting circuit 15, the subtracting circuit
 15 16, and the correction circuit 17a. The other structure of the DC bias control circuit is the same as that of the photo receiver of the first embodiment shown in Fig. 1, and the explanation of the same components designated by the same reference numerals will be omitted hereafter.

In operation, the High level detection circuit 11, the DC level detection circuit 12, and the Low level detection circuit 13 detect the High level, the DC level, and the Low level of the output signal of the amplifier 2a, respectively, like those of the photo receiver of the first embodiment. Furthermore,
 25 the subtracting circuit 14, the subtracting circuit 15, and the subtracting circuit 16 also determine the first subtraction result, the second subtraction result, and the third subtraction result, respectively, like those of the photo receiver of the first embodiment.

30 The correction circuit 17a weights ($\Delta V_{\text{high}} - \Delta V_{\text{low}}$) which

is the third subtraction result determined by the subtracting circuit 16 according to the input/output characteristics of the amplifier 2a, and then determines the difference ΔV between the level of the crossing point of the eye diagram of the output signal from the amplifier 2a, at which the rising and falling edges of pluses included in the output signal cross each other, and the DC level, so as to reduce the DC bias applied to the normal-phase side of the input of the data regeneration circuit 4a by only ΔV . Thus, the level of the crossing point of the eye diagram of the output signal from the amplifier 2a, at which the rising and falling edges of pluses included in the output signal cross each other, can be matched with the threshold voltage, or the difference between the level of the crossing point and the threshold voltage can be reduced.

As mentioned above, in accordance with the second embodiment, the DC bias control circuit detects a HIGH level, a DC level, and a LOW level of an output signal from an amplifier 2a, determines a first subtraction result by subtracting the DC level from the HIGH level, determines a second subtraction result by subtracting the LOW level from the DC level, determines a third subtraction result by subtracting the second subtraction result from the first subtraction result, and corrects a DC bias by weighting the third subtraction result according to characteristics of the amplifier 2a, so that the level of a crossing point of an eye diagram of the output signal from the amplifier, at which the rising and falling edges of pluses included in the output signal cross each other, is made to match with or be close to a threshold voltage of a data regeneration circuit 4a, even though the input signal has a distortion and the level of the crossing point is shifted from the mean level

of the input waveform. Accordingly, the present embodiment offers an advantage of being able to reduce the amount of jitter in regenerated data.

Many widely different embodiments of the present invention
 5 may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213